IN THE DRAWINGS:

The attached sheet of drawings include changes to Fig. 33B to add reference numerals 270-274. This sheet, which includes Figs. 33A, 33B replaces the original sheet and the prior replacement sheet.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

REMARKS

Applicant has the following response to the Office Action of June 23, 2005.

Drawings

Upon review of the application and drawings, Applicants discovered that page 73, lns. 1-4 of the specification, in discussing Fig. 33B, refers to reference numerals 270-274. These numerals were inadvertently left off of the drawing of Fig. 33B. Accordingly, Applicants are amending Fig. 33B to include such numerals. No new matter is being added.

Therefore, it is respectfully requested that this amendment to the drawings be entered and allowed.

Specification

Applicants also noticed a few informalities in the specification. Accordingly, Applicants are amending the specification to correct these informalities. No new matter is being added.

Accordingly, it is respectfully requested that these amendments to the specification be entered and allowed.

Claim Rejections - 35 USC §103

Claims 1-3, 8, 9, 35, 36, 41, 57 and 66

In the Office Action, the Examiner rejects Claims 1-3, 8, 9, 35, 36, 41, 57 and 66 under 35 USC §103(a) as being unpatentable over "Applicant's admitted prior art", Ohzu et al. (US publication 2002/0167601) and further in view of Houston (US 5,917,365). This rejection is respectfully traversed.

In the Office Action, the Examiner admits that the "admitted prior art" does not disclose an electric discharging transistor and an electric discharging power source wherein one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor, as recited in independent Claim 1, The Examiner, however, contends that Ohzu teaches an electric discharging transistor (fig. 5, element 38-1) and an electric discharging power source line wherein the output terminal is connected to a power source line and the electric discharging power source line is connected to a drain terminal of the electric discharging transistor in order to charge/discharge the capacitor and concludes that there is motivation to combine the "admitted prior art" with Ohzu to reduce image lag.

Applicants respectfully disagree. Ohzu merely discloses a transistor for charging/discharging a store capacitor. [0176] in Ohzu. There is no disclosure or suggestion in Ohzu of connecting it to an amplifying transistor and a biasing transistor (i.e. a source follower circuit, see page 6, lns. 5-7). Hence, Ohzu does not disclose or suggest that one of source and drain terminals of an electric discharging transistor is connected to the output terminal (the source terminal of the amplifying transistor).

The advantages of the semiconductor device of independent Claim 1 with an electric discharging transistor having the above structure are explained throughout the specification of the present application. For example, as explained on page 36, lns. 15-19, the claimed semiconductor device prevents the signal writing-in time from becoming too long, while enlarging the amplitude of the output electric potential and widening the operating region in which the input/output relationship is linear. When these objectives are achieved, the operation of the device will not become slow as in past devices and the quality of the image read from an image sensor is enhanced.

Similarly, the method of independent Claims 35 and 57 is not disclosed or suggested by the cited references. For example, each of these claims recites that the driving method outputs a signal after performing a pre-discharge. Claim 57 expands on that by stating that the driving method outputs a signal after performing a pre-discharge by making the electric discharging transistor into a conductive state. As explained in, for example, Embodiment Mode 2 on pages 41-45 of the present application, these features result in the signal writing-in being done in a short time. As explained above, this provides an inventive step and improvements over prior methods.

In addition, it is respectfully submitted that the cited disclosure in Houston is not relevant to the claimed invention. In particular, Houston merely discusses a threshold voltage without any disclosure or suggestion of a source follower circuit or an electric discharging transistor. Hence, one skilled in the art would not look to this reference to apply the cited disclosure to a source follower circuit or an electric discharging transistor, except by hindsight using the claims of the present application as a guide. As this is improper, the rejection based thereon is also improper.

Accordingly, it is respectfully submitted that independent Claims 1, 35 and 57, and those claims dependent thereon, are patentable over the cited references, and it is requested that this rejection be withdrawn.

Claims 10-14

The Examiner also rejects Claims 10-14 under 35 USC §103(a) as being unpatentable over applicants "admitted prior art," Ohzu, Houston in view of Silver et al. (US 6,690,842). This rejection is also respectfully traversed.

Each of these claims is a dependent claim. Therefore, for at least the reasons discussed above for the independent claims, these claims are also patentable. Accordingly, it is respectfully requested

that this rejection be withdrawn.

New Claims

Applicants are also adding new Claims 71-88 herewith. Independent Claims 71, 81 and 85 correspond to Claims 1, 35 and 57, respectively, but do not include the limitation of wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

These new claims are allowable over the cited references for similar reasons to those discussed above.

The new claims also include the feature of a transistor using a crystalline silicon film as the active layer. This is shown, for example, in Embodiment 3 of the specification of the present application.

Accordingly, it is respectfully requested that these new claims be entered and allowed.

The fee for new claims has been calculated as shown below.

	Claims Remaining After Amendment		Highest Number Previously Paid For	Present Extra	Rate	Fee
Total	33	-	24	9	(small entity) x 25 (others) x 50	$450.00
Independent	6	-	7	0	(small entity) x 100 (others) x 200	$0.00
Multiple Dependent (None)					(small entity) + 180 (others) + 360	$0.00
TOTAL ADDITIONAL FEES						$450.00

The undersigned authorizes the commissioner to charge our deposit account 50/1039 for the fee for these new claims.

Conclusion

Accordingly, it is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any further fee is due for this amendment, please charge our deposit account no. 50-1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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Fig. 33A

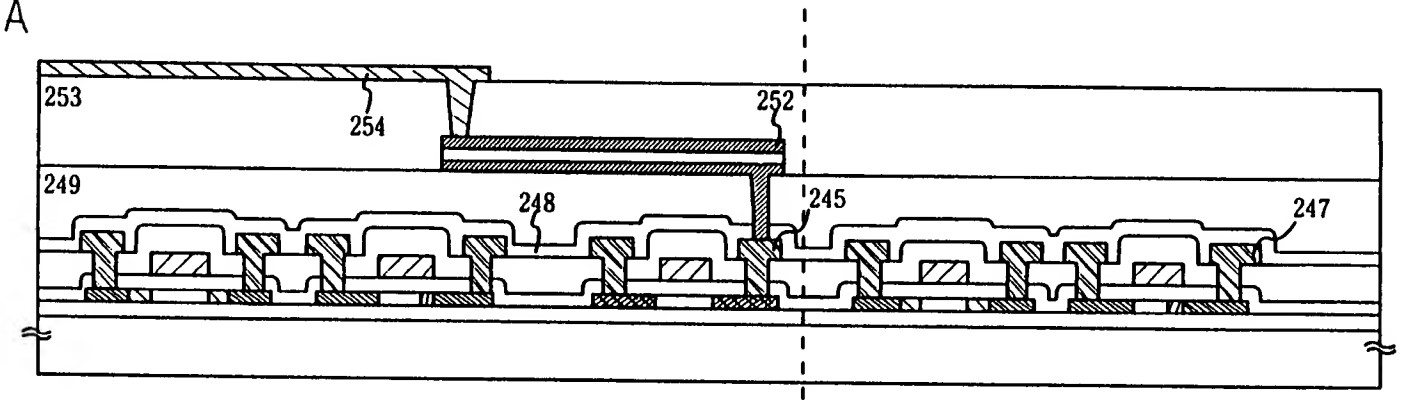

Fig. 33B